AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Original) A semiconductor device comprising:

a voltage node coupled to a first p-type region;

a first n-type region having a first side adjoining the first p-type region;

a second p-type region having a first side adjoining a second side of the first n-type region;

a second n-type region having a first side adjoining a second side of the second p-type region;

a clamping circuit intercoupled between the second n-type region and ground; and

a switching circuit intercoupled between the second p-type region and ground.

2. (Original) The device of claim 1, further comprising a resistive element intercoupled between the first n-type region and the voltage node.

3. (Original) The device of claim 2, wherein the resistive element comprises a resistor.

4. (Original) The device of claim 1, wherein the voltage node comprises a bond pad.

5. (Original) The device of claim 1, wherein the switching circuit comprises a resistor.

6. (Original) The device of claim 1, wherein the switching circuit comprises a transistor.

7. (Original) The device of claim 6, wherein the transistor comprises an NPN transistor.

8. (Original) The device of claim 6, wherein the transistor comprises an NMOS transistor.

9. (Original) The device of claim 1, wherein the clamping circuit comprises a transistor.

10. (Original) The device of claim 9, wherein the transistor comprises an NPN transistor.

11. (Original) The device of claim 9, wherein the transistor comprises an NMOS transistor.

12. (Original) The device of claim 1, wherein the clamping circuit comprises a diode.

13. (Withdrawn) A method of providing a semiconductor device utilizing a silicon controlled rectifier, the method comprising the steps of:

providing a semiconductor device having a silicon controlled rectifier formed therein;

providing a clamping structure, coupled to the silicon-controlled rectifier, adapted to prevent a p-n junction within the silicon controlled rectifier from retaining a forward bias;

providing a switching structure, coupled to the p-type portion of the p-n junction and adapted to ground the p-type portion during normal operation of the semiconductor device.

14. (Withdrawn) The method of claim 13, wherein the step of providing the switching structure comprises providing a resistor.

15. (Withdrawn) The method of claim 13, wherein the step of providing the switching structure comprises providing a transistor.

16. (Withdrawn) The method of claim 15, wherein the step of providing the transistor further comprises providing an NPN transistor.

17. (Withdrawn) The method of claim 15, wherein the step of providing the transistor further comprises providing an NMOS transistor.

18. (Withdrawn) The method of claim 13, wherein the step of providing the clamping structure comprises providing a diode.

19. (Withdrawn) The method of claim 13, wherein the step of providing the clamping structure comprises providing a transistor.

20. (Withdrawn) The method of claim 19, wherein the step of providing the transistor further comprises providing an NPN transistor.

21. (Withdrawn) The method of claim 19, wherein the step of providing the transistor further comprises providing an NMOS transistor.

22. (Original) A system for providing a electrostatic discharge protection in a semiconductor device, utilizing a silicon controlled rectifier, the system comprising:

a silicon controlled rectifier having a first p-type region coupled to a voltage node, a first n-type region having a first side adjoining the first p-type region, a second p-type region having a first side adjoining a second side of the first n-type region, and a second n-type region having a first side adjoining a second side of the second p-type region;

a clamping structure, intercoupled between the second n-type region and ground, and adapted to prevent the junction between the second p-type region and the second n-type region from retaining a forward bias ; and

a switching structure, intercoupled between the second p-type region and ground, and adapted to ground the second p-type region during normal operation of the semiconductor device.